AMENDMENTS

In The Specification:

Please amend paragraph [0001] as follows:

[0001] The present invention relates to a charge pump and a voltage doubler using the same. More particularly, the present invention relates to a charge pump comprising low-pressure fabricated metal-oxide-semiconductor (MOS) devices and a voltage [[~~double~~]]doubler using the same.

Please amended paragraph [0007] as follows:

[0007] A voltage doubler that uses this type of charge pump was first disclosed in the article 'A High-Efficiency CMOS Voltage Doubler' of the IEEE Journal of Solid State Circuits, Vol. 33, No. 3, March 1998 by Philippe Deval and Mechel J. Declercq. Fig. 1B is a circuit diagram of the voltage doubler that uses the conventional charge pump design shown in Fig. 1A. The clocking signal CK varies cyclically between V_{IN} and 0V during operation. Hence, the output voltage V_{OUT} approaches $2*V_{IN}$. Similarly, the gate-substrate interface of the NMOS transistors 122 and 124 must be able to sustain a voltage difference of at least $2*V_{IN}$. In Fig. 1B, a clock signal CK is connected to a terminal 132b of the capacitor 132. The another terminal 132a of the capacitor 132 is connected to the NMOS transistors 122. Similarly, an inverted clock signal CK' is connected to a terminal 134b of the capacitor 134. The another terminal 142a of the capacitor 134 is connected to the NMOS transistors 124. In addition, the PNOS transistors 140, 142, 144, and 146 form a circuit, as shown in Fig. 1B, which has two terminals

coupled to the terminals 132a and 134a and a voltage output terminal V_{out}. The voltage output terminal is also coupled to a ground via a capacitor 152. In addition, all the substrates of the PNOS transistors 140, 142, 144, and 146 are coupled to the ground via a capacitor 150.

Please amend paragraph [0027] as follows:

[0027] Fig. 3 is a block diagram showing the circuit of a voltage doubler according to one preferred embodiment of this invention. In Fig. 3, the charge pump structure and operating method is similar the one shown in Fig. 2 and hence detailed description is omitted. In general, the largest voltage from the output terminals V_{OUT1} and V_{OUT2} is roughly twice that of the input voltage V_{IN}. Hence, voltage doubling is obtained if the output voltage switching unit 340 picks up the one having the highest voltage to be the output voltage at the output terminal V_0 among the output terminals V_{OUT1} and V_{OUT2}. In Fig. 3, the charge pump circuit 32, like in Fig. 2, includes two capacitors 330 and 332. One end of the capacitor 330 receives the clocking signal CK while the other end of the capacitor 330 couples electrically to the first output terminal 220 of the output voltage generation unit 206. Meanwhile, the first output voltage at the first output terminal 220 is output from the output terminal V_{OUT1}. Similarly, one end of the capacitor 332 receives the inverted clocking signal CK' while the other end of the capacitor 332 couples electrically with the second output terminal 322 of the output voltage generation unit 308. The second output voltage at the second output terminal 322 is output from the output terminal V_{OUT2}. The control signal generation units 302 and 304 are similar to the control signal generation units 202 and 204 in Fig. 2.

Please amend paragraph [0040] as follows:

[0040] Fig. 5 is an actual circuit diagram of a voltage doubler according to another preferred embodiment of this invention. As shown in Fig. 5, the charge pump 52 is structurally similar to the one in Fig. 4 and hence detailed description of its operation is not repeated here. The elements of 502-508, 512-518, 530 and 540 are similar to the elements 402-408, 412-418, 430, and 440 in FIG 4. The charge pump 52 with an application as an example has output terminals similar to the first output terminal V_{OUT1} and the second output terminal V_{OUT2} as shown in Fig. 4, and numbered in Fig. 5 as 550 and 552, respectively. In the same way, when the voltage of the clocking signal and the inverted clocking signal oscillates between 0 [[~]]and V_{IN}, voltage at the first output terminal V_{OUT1} and the second output terminal V_{OUT2} oscillates at a voltage between V_{IN} [[~]]and $2*V_{IN}$. In the following, operation of the circuit outside the charge pump 52 is explained in detail.

Please amend paragraph [0042] as follows:

[0042] In addition, one source/drain terminal (or the first source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 (or the seventh PMOS transistor) is electrically connected to the second output terminal V_{OUT2}. The other source/drain terminal (or the second source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to a final output terminal 590 for outputting a final output voltage V_0. The substrate (or the substrate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the substrate and source/drain terminal of the PMOS transistor 562. The gate (or the gate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the first output voltage terminal V_{OUT1}. One source/drain terminal (or the first

source/drain terminal of the eighth PMOS transistor) of the PMOS transistor 568 (or the eighth PMOS transistor) is electrically connected to the first output voltage terminal V_{OUT1}. The other source/drain terminal (or the second source/drain terminal of the eighth PMOS transistor) of the PMOS transistor [[~~586~~]]568 is electrically connected to the final output terminal 590. The substrate (or the substrate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the substrate of the PMOS transistor 564. The gate (or the gate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the second output voltage terminal V_{OUT2}.

In The Drawings:

Applicant amends specification instead of further amending drawings.